center for technology transfer and innovation
at the Jožef Stefan Institute

Jožef Stefan Institute, Ljubljana, Slovenia

Innovative superconductor-based memory device and method for its operation, using a switchable resistive element suitable for superconducting computing -

compatible with superconducting flux-quantum electronics

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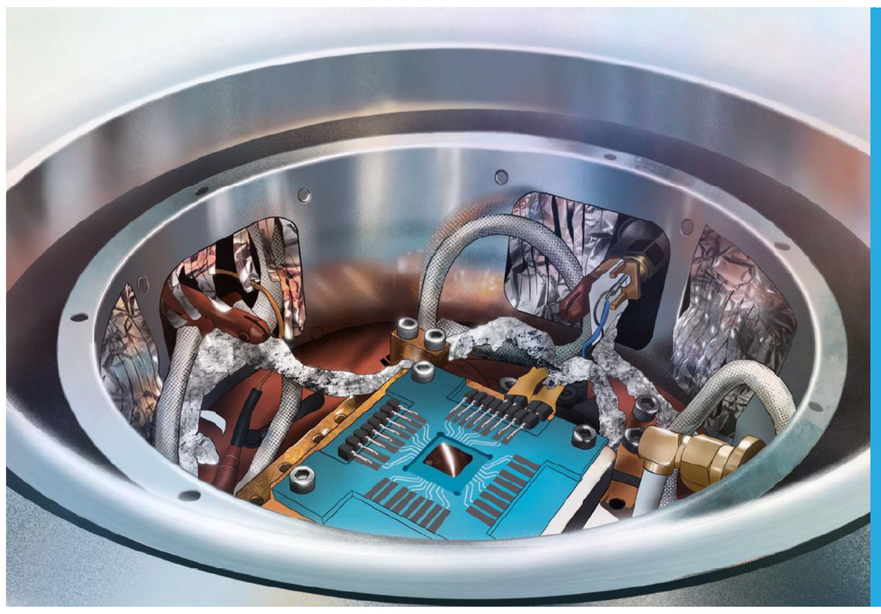
A new device and method for its operation has been developed by researchers from Slovenia. Developing a superconducting computer that could outperform conventional computers with high speed and low power consumption has been a desirable goal for a long time. One of the remaining obstacles still is the development of a fast, scalable, low power memory. An example of a known proposal for a memory solution is a superconducting-nanowire memory element operated by nanowire cryotrons. Various hybrid devices also have been developed in the past. Here, a memory device that combines a switchable resistive element, with a superconductor element to control the switching, is proposed.



Picture from Jožef Stefan Institute
(JSI, F7 - The department of Complex Matter).
Artistic rendering performed by Superconductor Week
(USA) www.superconductorweek.com

Technology field: computer hardware, semiconductors, quantum electronics, nanotechnologies related to electronics & microelectronics.

The memory device consists of a narrow channel made of a memristive nonvolatile charge density wave (CDW) material. The memristive non-volatile CDW material may be referred to as a switchable resistive element. The normal state after cooling down to cryogenic temperature is high resistance state. Above a certain current threshold, the resistive element is caused to undergo a transition to the low resistance state which constitutes the Write operation. The reverse transition from the low resistance state to the high resistance state of the memristive element (the Erase operation) is caused when the current exceeds a certain but different value of critical current, changing the shunt resistance to a high value. The superconducting memory device described may be in the form of a nanowire or a three-terminal device such as nano-cryotron (nTron) device. The suitable device operating temperature is 40 K or lower. The width of the device is few tens of nm enabling high scalability.

Advantages:

A hybrid superconducting memory device proposed combines a superconductor element in parallel with a switchable resistive element. The proposed device is characterized by:

- ultrafast switching speed <40 ps,
- two- or three-terminal operation,
- scalability, ultralow switching energy (due to the ability to use lowenergy memristive elements) <0.25 pJ/bit,
- low-temperature operation,
- ease of integration, simple circuit design and compatibility with superconducting flux-quantum electronics.

STAGE OF DEVELOPMENT

Technology is developed at Concept stage and is available for demonstration.

TARGET SECTORS

Manufacturers of superconductors, computer components, quantum computing and other related devices are sought for license agreement.

INTELLECTUAL PROPERTY

Patent pending.

CONTACT DETAILS

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