FAMES Pilot Line

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TOPIC : Description of the FAMES Pilot Line project, coordinated by CEA

Summary

The FAMES Pilot Line provides a complete toolbox of technologies for developing innovative chips architecture increasing performance and lowering power consumption of mixed-signal circuits.

The project aims to strengthen European sovereignty in microelectronics by advancing semiconductor technologies, focusing on developing FD-SOI[1] technologies at 10nm and 7nm nodes, eNVM[2] solutions, RF components, 3D integration, and PMIC[3] technologies.

The FAMES Pilot Line will provide an Open Access for EU stakeholders, including academic teams, SMEs and large companies and offer training opportunities to foster skilled talent. Industrial support from major companies such as ASML, Nokia, Ericsson, Siemens, Soitec and STMicroelectronics highlights the importance of the FAMES Pilot Line.

FAMES Pilot Line project developed in the frame of the EU Chips Act

FAMES (FD-SOI Pilot Line for Applications with embedded non-volatile Memories, RF, 3D integration & PMIC, to ensure European Sovereignty) has been elaborated to address the Operational Objective 2 of the European Chips Act - Pillar 1: “Enhancing existing and developing new advanced pilot lines across the EU”.

The FAMES Pilot Line consortium, led by CEA-Leti (France), is composed of four Hosting Sites (CEA-Leti in Grenoble/France, Tyndall in Cork/Ireland, VTT in Espoo/Finland and Silicon Austria Labs (SAL) in Villach/Austria) that will operate collaboratively a distributed Pilot Line and collectively integrate a set of new semiconductor equipment (300mm) in addition to their respective existing infrastructures. FAMES Pilot Line consortium also includes 7 additional partners, with renowned RTOs (Imec (Belgium), Fraunhofer (Germany)), Universities (Cezamat WUT (Poland), Université Catholique de Louvain (Belgium), University of Granada (Spain) and Grenoble INP (France)) and the SiNano association (based in Grenoble, France) to develop an ambitious R&D program.

With a total budget of €830 million allocated until December 2028, evenly co-funded by the EU and participating Member States, the FAMES Pilot Line will strengthen the European microelectronics ecosystem.

[1] Fully Depleted-Silicon-on-Insulator
[2] Embedded Non-Volatile Memories
[3] Power Management Integrated Circuit

FAMES Pilot Line main objectives

The first objective of the FAMES Pilot Line is to offer a set of advanced technologies with two new generations of FD-SOI technology at 10nm and 7nm nodes, eNVM solutions embedded in metallic interconnects above transistors, radiofrequency (RF) components (passives, switches, and filters), 3D stacking options (3D sequential integration and 3D heterogeneous integration) and magnetic inductances for PMIC.

The second objective of the FAMES Pilot line is to promote and provide open access to this Pilot Line to a diverse range of stakeholders of the electronic value chain such as academic research teams, SMEs, start-ups or large industrial groups (materials and equipment suppliers, OEMs[4], foundries, IDMs[5], EDA[6] vendors, fabless companies). This access will give Europe the opportunity to explore a wide spectrum of semiconductor markets, strengthening European leadership and opening up new opportunities.

Finally, the FAMES Pilot Line project will develop training activities at Master and PhD levels, so that students and young researchers can acquire advanced skills in the technologies developed on the FAMES Pilot Line.

The project has received 43 letters of support from industrial companies covering all the electronic systems value chain, including Nokia, Ericsson, Nordic, Soitec, ASML, ASM, AMAT, GlobalFoundries, IBM, Intel, STMicroelectronics, Siemens, Orange, Meta, Stellantis, Valeo and many more. This overwhelming support shows that the FAMES Pilot Line is gathering significant interest from industry.

FAMES Pilot Line opens the door for disruptive chips architectures around FD-SOI technology

All technologies developed in the FAMES Pilot Line will enable new chip architectures delivering robust performance enhancements and substantial efficiency gains, fulfilling Users' requirements and sustainably supporting the massive digitalization of our society. The FAMES Pilot Line will drive eco-friendly practices by prioritizing resource optimization, advocating for a circular economy, and minimizing waste across the entire technological process, from chip design to manufacturing. As such, it will significantly bolster the industry's pursuit of achieving net-zero emissions by 2050 (objective of the EU Green Deal).

The FD-SOI technology (invented, fully patented, and developed in Europe, and well suited to reinforce European industrial strengths) has been supported by numerous EU collaborative project frameworks (ENIAC, ECSEL, KDT, CHIPS) involving many academic and industrial partners. These projects have strongly contributed to create a robust and comprehensive ecosystem. Most of the FD-SOI value chain (wafer manufacturing, modelling, chip design and process, etc.) is mastered and hosted in Europe. Soitec is a world leader in FD-SOI substrate wafers manufacturing, STMicroelectronics (ST) and GlobalFoundries (GF) use Soitec's wafers to process 28nm and 22nm FD-SOI Integrated Circuits in Europe. Leading global companies such as Qualcomm, Google, Samsung, Sony, Bosch, Nordic, NXP and

[4] Original Equipment Manufacturer
[5] Integrated Device Manufacturer
[6] Electronic Design Automation : software tools to design chips and semiconductor devices

STMicroelectronics use FD-SOI technology in their products. Given the growing adoption of FD-SOI technology by the industry, pursuing the technology roadmap with the two new generations proposed in the FAMES Pilot Line has become a necessity.

The FAMES Pilot Line will be able to serve applications that go far beyond the purely digital domain, and it will be a key enabler for a whole range of More than Moore[7] devices and related applications. The FAMES Pilot Line capabilities and expertise will facilitate the prototyping of core functions including sensors, actuators and transmission functions for a wide range of devices. Technologies proposed will allow new generations of microcontrollers, microprocessor units, chips for 5G/6G, smart imagers, smart sensors, processors for data fusion, wearable devices, trusted chips, quantum and cryoCMOS, edge AI chips and advanced packaging with chiplets, to name a few.

Value proposition for Industrial and Research partners from EU Member States

FAMES Pilot Line will be a one-stop shop with open access for all EU stakeholders, and will set up a dedicated team to provide Open Access mechanisms to Users from all EU or like-minded countries. These Users from Research and Industry will have access to R&D services through two open access modes:

1) A reactive mode in which the FAMES consortium will assess the feasibility of User spontaneous requests to access the FAMES Pilot Line;

2) A proactive mode with an annual open call for Users to request access to design and modelling tools via PDK distribution, to evaluate FAMES Pilot Line technologies: 1) FD-SOI 10nm and 7nm technology; 2) embedded non-volatile memories; 3) RF components; 4) 3D options, and 5) PMIC and 6) specific demonstrator results;

Therefore, the FAMES Pilot Line could be leveraged by EU research teams and industry partners to:

- Use FAMES technology results to further develop customized solutions to address company specific needs;
- Leverage FAMES Pilot Line unique capability to test FD-SOI specific circuit designs through MPWs[8] opportunities;
- Develop innovative designs by using various PDKs provided by the FAMES Pilot Line;
- Generate new IP through advanced developments based on the technology results of the FAMES Pilot Line;
- Get inspired by demonstrators results and imagine new solutions for specific markets;
- Learn more about FAMES-related technologies to educate high-value skill forces and get involved in the FD-SOI European ecosystem.

[7] "More than Moore" is a functional diversification incorporating functionalities that are more than digital and analog signals and architectures used in conventional semiconductors.

[8] MPW or Multi-Project Wafers semiconductor manufacturing allow customers to share tooling (such as masks) and microelectronics wafer fabrication costs between several designs or projects (Wikipedia)